several D flip-flops and DACs, one per data line. In this configuration, the processed pixel clock 117 is used to latch the video data signal 121 through to the RGB DAC 129.--

The paragraph beginning at line 23 of page 7 has been amended as follows:

--The clock phase selector 131 selects the proper clock phase for its two clock outputs so that the appropriate flip-flops (127 and 133) operate with proper setup and hold times. There are several options for implementing the clock phase selector 131. For instance, if the delay of the total clock path is predictable and within a small range, then a simple fixed value delay line can be implemented for the phase selector. This option has the advantage of being low cost. Alternatively, a coarse phase selector could be used to compare two local pixel clocks, 0 and 180 degrees, and pick the one that provides the best setup and hold time margins for the re-synchronization flip-flops. This method may be preferred for most applications. Yet another alternative is to use a phase-locked-loop (PLL) to develop the correct timing for the resynchronization flip-flops, resulting in the best setup and hold time margins. The PLL could be a simple phase-only tracking circuit. This approach offers finer phase steps than the coarse phase selector.--

In the Claims

Please cancel Claim 8.

Please amend Claims 1 and 7 as follows:

1. (Amended) A method for clocking video data to reduce beat patterns, comprising:

receiving a video data signal having a predetermined pixel frequency based on an external clock reference, the video data signal being provided by video data signal circuitry; and

providing a local clock signal to re-clock the video data signal between the video data signal circuitry and output circuitry, the local clock signal being based on the external clock reference, thereby removing interfering influence of other clock signals on the predetermined pixel frequency.